dust networks™

SmartMesh® IP

LTP5901/LTP5902-IPM

2.4 GHz 802.15.4 Eterna™ Mote Modules

About SmartMesh IP

Dust Networks' new standards-based SmartMesh® IP product line achieves unsurpassed levels of networking resilience and reliability, with advanced network management and comprehensive security. Based on Dust's breakthrough Eterna™ SoC technology, SmartMesh IP enables up to 8 times lower power consumption than competing solutions even in harsh, dynamically changing RF environments. Cost effective, Internet Protocol (IP) compatible, and widely applicable, SmartMesh IP serves an extensive range of applications, such as energy management, building automation, renewable energy, and other implementations in smart infrastructure that call for ultra low power.

Product Descriptions – LTP5901/LTP5902-IPM

SmartMesh IP networks are built from wireless network nodes called motes. The motes include advanced hardware and advanced software algorithms that provide resilient, reliable, and low-power true-mesh networks. Dust motes deliver unprecedented low power consumption with a receive current of less than 5 mA and a transmit current of less than 10 mA at +8dBm (< 6 mA at 0 dBm). With Dust's time-synchronized SmartMesh IP networking, all motes in the network may route and may be battery-powered, powered by an energy-harvester, or line powered. SmartMesh IP's time-synchronized mesh networking combines with Dust Network's innovative IEEE 802.15.4-compliant radio design to enable battery life of up to a decade for all motes, including routing motes, on two AA batteries.

The LTP5901/LTP5902-IPM Mote modules combine Dust Networks' robust sensor networking solution with Dust's breakthrough Eterna™ SoC Technology in an easy-to-integrate surface-mount printed circuit board (PCB). The LTP5901-IPM module includes an on-board chip antenna, while the LTP5902-IPM module includes an MMCX antenna connector. Both PCB modules will come with modular certifications for FCC, CE, and IC. Dust Networks provides a fully engineered RF solution, comprehensive APIs, and complete development documentation thereby accelerating customer development and reducing customer development costs.

Key Product Features

Highly Scalable

- Automatic network formation—new motes join automatically from anywhere in the network
- All motes are wireless routers, providing a full-mesh network that easily scales to tens of thousands of motes per square kilometer
- Time-synchronized communication across 15 channels virtually eliminates in-network collisions, allowing for dense deployments in overlapping radio space

Superior Reliability

- Intelligent Networking Platform enables greater than 99.99% network reliability even in the most challenging monitoring and control environments
- Time-synchronized channel hopping seamlessly compensates for in band blocking and multipath fading in dynamic RF environments

IP Standards Compliance

- Compliant to IETF 6LoWPAN and IEEE 802.15.4e standards

Ultra-low Power Operation

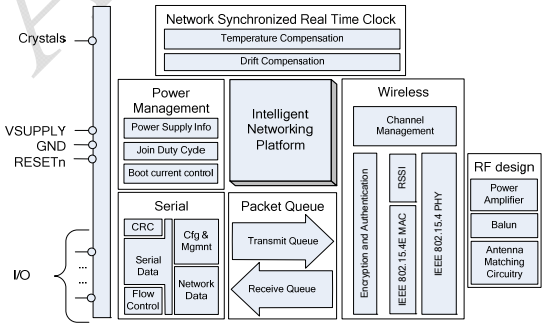
- Industry-leading radio technology capable of line-powered, battery-powered, or energy-scavenging operation
- Automatic power optimization of every device in network, enabling a decade of network operation on two Lithium AA batteries

Easy to Integrate and Deploy

- Fully engineered RF transceiver, with power amplifier (PA), integrated balun, and antenna matching circuitry
- Options for chip antenna or MMCX antenna connector
- A comprehensive application programming interface (API) provides a rich and flexible functionality to ease software development and device integration

Secure Global Market Solution

- Operates on 2.4 GHz global license-free band, providing customers with a single product for world-wide use
- RF modular certifications (pending)-FCC, IC, and CE
- AES-128 bit encryption



LINEAR TECHNOLOGY

Table of Contents

1.0 General

1.1 Related Documentation

- 040-0102 Eterna Integration Guide
- 040-0109 Design Specific Configuration Guide
- 040-0110 Eterna Serial Programmer Guide

1.2 Conventions

1.2.1 Signal Naming

The naming convention for Eterna signals is UPPER_CASE_SEPARATED_BY_UNDERSCORE. Active-low signals, such as RESETn, add a trailing lower case n. An exception to the naming convention is UART transmit and receive signals which are named consistent with industry practice as RX and TX, omitting the lower case n, despite being active low signals. The terms assertion and active refers to a signal in a logically true state: logic '1' for active high signals and logic '0' for active low signals. The terms negated and inactive refer to a signal being in its logically false state: logic '0' for active high signals and logic '1' for active low signals.

1.2.2 Number Format

The **0x** prefix indicates a hexadecimal number follows.

The **0b** prefix indicates a binary number follows.

The lack of a prefix indicates a decimal number follows.

2.0 Introduction

Eterna is the world's most energy-efficient IEEE 802.15.4 compliant platform enabling battery and energy harvested endpoint, routing and network management solutions. With a powerful 32-bit ARM® Cortex™-M3, best in class radio, flash, RAM and purpose-built peripherals, Eterna provides a flexible, scalable and robust networking solution for applications demanding both minimal energy consumption and data reliability in even the most challenging RF environments.

Shown in Figure 1, Eterna integrates purpose-built peripherals that excel in both low operating-energy consumption and the ability to rapidly and precisely cycle between operating and low-power states. Items in the shaded region correspond to the analog/RF components.

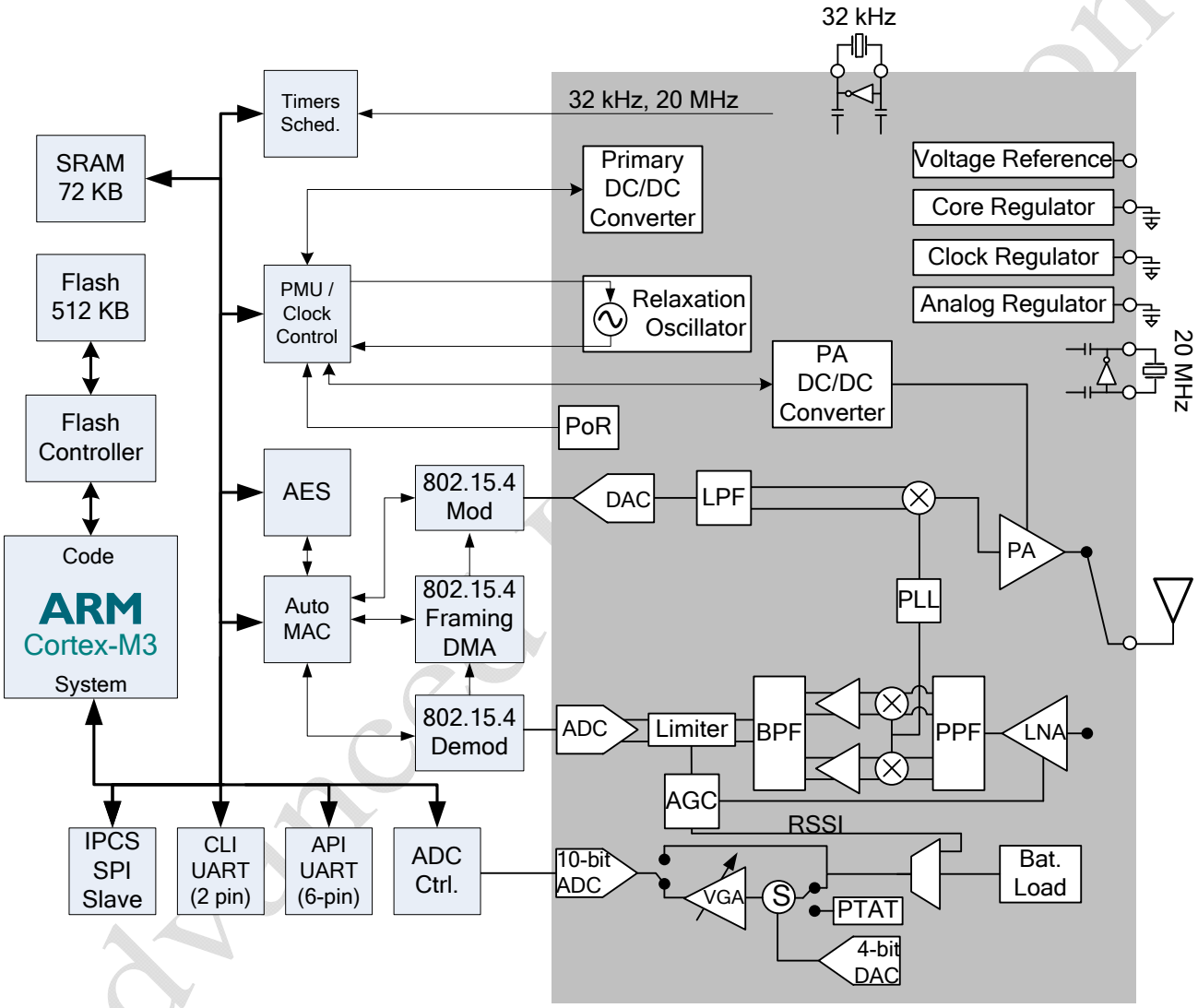


Figure 1 Eterna Block Diagram

2.1 Power Supply

Eterna is powered from a single pin, VSUPPLY, which powers the I/O cells and is also used to generate internal supplies. Eterna's two on-chip DC/DC converters minimize Eterna's energy consumption while the device is awake. To prevent power from being wasted the DC/DC converter is disabled when the device is in low-power state. Eterna's rejection of supply noise is substantial owing to the two integrated DC/DC converters and three integrated low-dropout regulators. Eterna's operating supply range is high enough to support direct connection to Li-$SClO_2$ sources and wide enough to support battery operation over a broad temperature range.

2.1.1 Supply Monitoring and Reset

Eterna integrates an Power on Reset (PoR) circuit and as the RESETn input pin is nominally configured with an internal pull-up resistor, thus no connection is required. For a graceful shutdown, the software and networking layers be cleanly halted prior to assertion of the RESETn pin. Eterna includes a soft brown-out monitor that fully protects the Flash from corruption in the event that power is removed while writing to flash. Integrated flash supervisory functionality in conjunction with *** (do we do a JFS?) yields a robust non-volatile file system.

2.2 Precision Timing

Eterna, differs from competing 802.15.4 product offerings by providing low-power dedicated timing hardware and timing algorithms that provide timing precision two to three orders of magnitude better than any other available low-power solution. Improved timing accuracy allows motes to minimize the amount of radio listening time required to ensure packet reception thereby lowering even further the power consumed by an Eterna network. Eterna's patented timing hardware and timing algorithms provide superior performance over rapid temperature changes, further differentiating Eterna's reliability when compared with other wireless products. In addition, precise timing enables networks to reduce spectral dead time, increasing total network throughput.

2.2.1 Time Synchronization

In addition to coordinating timeslots across the network, which is transparent to the user, Eterna's unparalleled timing management is used to support two mechanisms to share network time. Having an accurate, shared, network-wide time base enables events to be accurately time stamped or tasks to be performed in a synchronized fashion across a network. Eterna will send a time packet through its serial interface when one of the following occurs:

- Eterna receives an HDLC request to read time
- The TIMEn signal is asserted

The use of TIMEn has the advantage of being more accurate. The value of the timestamp is captured in hardware relative to the rising edge of TIMEn. If the HDLC request is used, due to packet processing the value of the timestamp may be captured several milliseconds after receipt of the packet. See Section 8.10 for the time functions definition and specifications.

2.3 Time References

Eterna includes three clock sources: a low power oscillator designed for a 32.768 kHz crystal, the radio reference oscillator designed for a 20 MHz crystal, and an internal relaxation oscillator.

2.3.1 Relaxation Oscillator

The relaxation oscillator is the primary clock source for Eterna, providing the clock for the CPU, memory subsystems, and all peripherals. The internal relaxation oscillator typically starts up in a few µs, providing an expedient, low-energy method for duty cycling between active and low power states. Quick start-up from the doze state, defined in section 4.0, allows Eterna to wake up and receive data over the UART and SPI interfaces by simply by detecting activity the appropriate signals.

2.3.2 32.768 kHz Crystal

Once Eterna is powered up and the 32.768 kHz crystal source has begun oscillating, the 32.768 kHz crystal remains operational while in the Active state, and is used as the timing basis when in Doze state. See Section 4.0 for a description of Eterna's operational states.

2.3.3 20 MHz Crystal

The 20 MHz crystal source provides a frequency reference for the radio, and is automatically enabled and disabled by Eterna as needed.

2.4 Radio

Eterna is the lowest-power commercially available 2.4 GHz IEEE 802.15.4e radio by a substantial margin. (Please refer to section 8.2 for power consumption numbers.). Eterna's integrated power amplifier is calibrated and temperature-compensated to consistently provide power at a limit suitable for worldwide radio certifications. Additionally, Eterna uniquely includes a

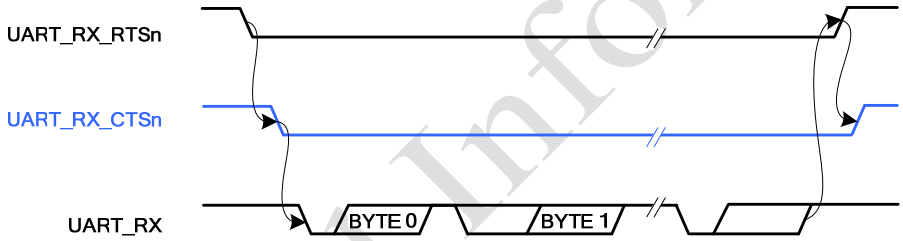
hardware-based autonomous MAC that handles precise sequencing of peripherals, including the transmitter, the receiver, and AES peripherals. The hardware-based autonomous MAC minimizes CPU activity, thereby further decreasing power consumption.

2.5 UARTs

The principal network interface is through the application programming interface (API) UART. A command-line interface (CLI) is also provided for support of test and debug functions. Both UARTs sense activity continuously, consuming virtually no power until data is transferred over the port and then automatically returning to their lowest power state after the conclusion of a transfer.

2.5.2 API UART Protocol

Eterna's API UART operates in Mode 4, incorporating optional flow control, at 115200 baud. Packets are HDLC encoded with one stop bit and no parity bits. The flow control signals for Eterna's API receive path are shown in Figure 5. If the flow control signals are used (recommended) transfers are initiated from a companion processor by asserting UART_RX_RTSn. Eterna responds by asserting UART_RX_CTSn. If flow control is used, after detecting the assertion of UART_RX_CTSn the companion processor may send the entire packet. Following the transmission of the final byte in the packet the companion processor negates UART_RX_RTSn and waits until the negation of UART_RX_CTSn before asserting UART_RX_RTSn again. Flow control automatically ensures compliance with inter-packet delay requirements, so explicit delay-checking is not required.



If flow control is not desired or needed it may be disabled by tying UART_RX_RTSn high. When flow control is not used the companion processor may send the entire packet; in this case the companion processor must comply with the minimum inter-packet delay as defined in section 8.9.

Figure 5 UART Mode 4 Receive Flow Control

UART Mode 4 also incorporates level-sensitive flow control for Eterna UART transmissions on the UART TX pin. Packets are HDLC encoded with one stop bit and no parity bits. The flow control signals for TX are shown in Figure 6. A transfer request is signaled by Eterna device asserting UART_TX_RTSn. The UART_TX_CTSn signal may be actively driven by the companion processor when it is ready to receive a packet or it may be tied low if the companion processor will always be ready to receive a packet. After detecting a logic '0' on UART_TX_CTSn Eterna sends the entire packet. Following the transmission of the final byte in the packet Eterna negates UART_TX_RTSn and waits for a minimum period (what is the period called?) defined in section 8.9 before asserting UART_TX_RTSn again (if a packet needs to be transmitted)

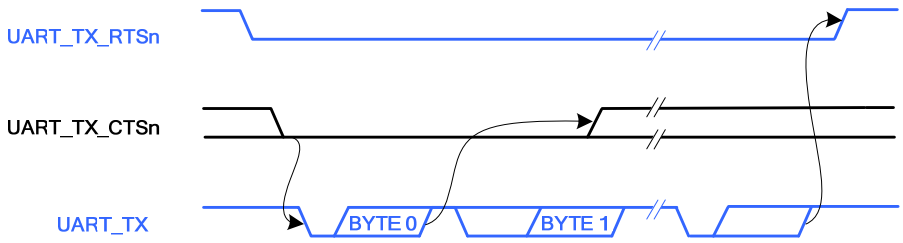


Figure 6 UART Mode 4 Transmit Flow Control

For details on the timing of the UART protocol, see section 8.9 (UART AC Characteristics).

2.5.3 CLI UART

The Command Line Interface (CLI) UART port is a two wire protocol (TX and RX) that operates at a fixed 9600 baud rate with one-stop bit and no parity. The CLI UART interface is intended to support command-line instructions and response activity.

2.6 Autonomous MAC

Eterna was designed as a system solution with the objective of providing a reliable, ultra-low power, and secure network. A reliable network capable of dynamically optimizing operation over changing environments requires solutions that are far too complex to completely support through hardware acceleration alone. As described in Section 2.2, proper time management is essential for optimizing a solution that is both low power and reliable. To address this solution Eterna includes the Autonomous MAC, which includes hardware support for controlling all of the time-critical radio operations. The Autonomous MAC provides two benefits: first, preventing variable software latency from affecting network timing and second, greatly reducing system power consumption by allowing the CPU to remain inactive during the majority of the radio activity. The Autonomous MAC, unique to Eterna, provides software-independent timing control of the radio and radio-related functions, resulting in superior reliability and exceptionally low power.

2.7 Security

Network security is an often overlooked component of a complete network solution. Proper implementation of security protocols is significant in terms of both engineering effort and market value in an OEM product. Eterna system solutions provide a FIPS-197 validated encryption scheme, and goes further, providing a complete set of mechanisms to protect network security. Eterna includes hardware support for electronically locking devices, thereby preventing access to Eterna's flash and RAM memory. This lock-out feature provides a means to securely unlock a device should support of a product require access. For details see 040-0109 Design Specific Configuration Guide.

2.8 Temperature Sensor

Eterna includes a calibrated temperature sensor on chip. The temperature readings are available locally through Eterna's serial API, in addition to being available via the network manager. The performance characteristics of the temperature sensor can be found in Section 8.6.

2.8.1 Radio Inhibit

The RADIO_INHIBIT digital interrupt enables an external controller to temporarily disable the radio software drivers (for example, to take a sensor reading that is susceptible to radio interference). When RADIO_INHIBIT is asserted the software radio drivers will disallow radio operations including clear channel assessment, packet transmits, or packet receipts. If a radio event is in progress radio inhibit will take effect after the present operation completes. For details on the timing associated with RADIO_INHIBIT, see Section 8.12.

2.8.2 Sleep

The SLEEPn digital interrupt enables an external controller to temporarily disable Eterna's duty cycling between active and Doze states (see Section 4.0 for state definitions). Forcing Eterna to the Doze state should only be done when absolutely necessary, such as when taking a very sensitive sensor reading, as forcing a device into a Doze state will on the average increase the energy consumption of other devices in the network. When SLEEPn is asserted the software will go into a Doze state until the SLEEPn signal is negated. For details on the timing associated with SLEEPn, see Section 8.11.

2.10 Flash Programming

Eterna's software images are loaded via the IPCS, in-circuit programming control system, SPI interface. Sequencing of RESETn and FLASH_P_ENn, as described in Section 4.0, places Eterna in a state emulating a serial flash to support in-circuit programming. Hardware and software for supporting development and production programming of devices is described in 040-0110 Eterna Serial Programmer Guide. The serial protocol, SPI, and timing parameters are described in Section 8.13.

4.0 Operation

In order to provide capabilities and flexibility in addition to ultra low power, Eterna operates in various states, as shown in Figure 8 and described in this section.

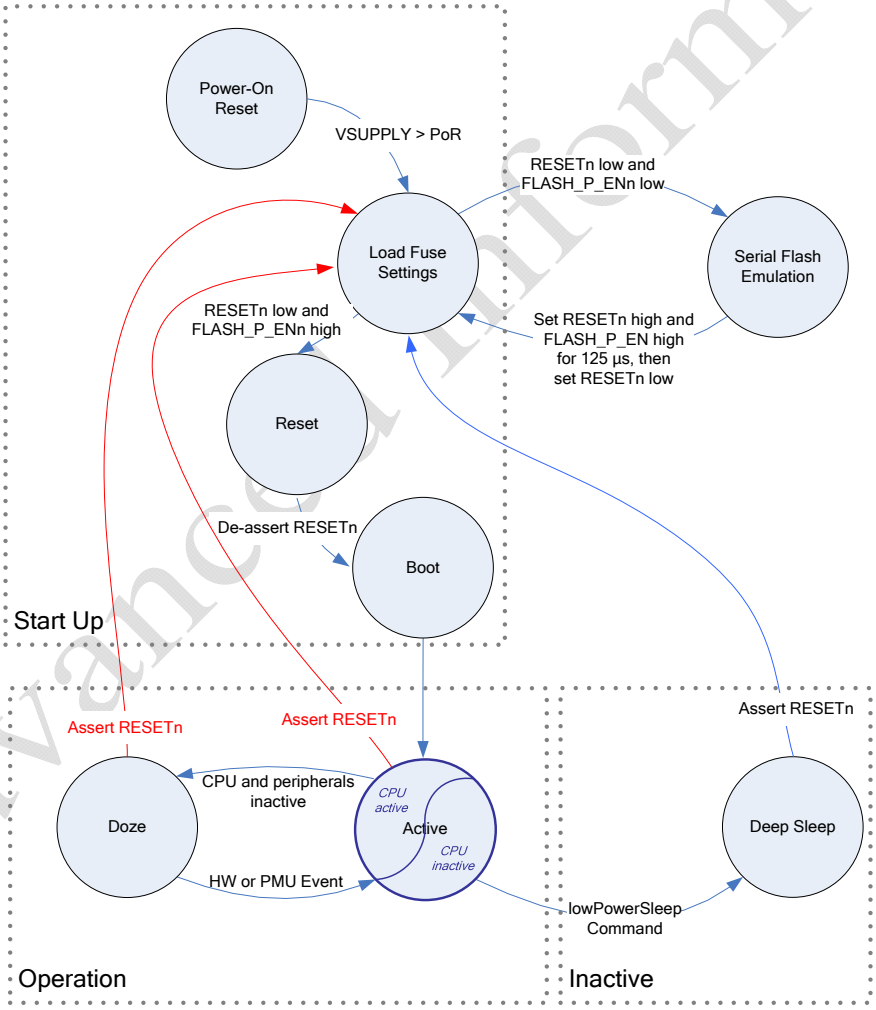


Figure 8 State Diagram – Operating Modes

4.1 Start Up

Start Up occurs as a result of either tripping of the power-on-reset circuit or the assertion of RESETn. After the completion of power-on-reset (see Section 2.1.1) or the falling edge of an internally synchronized RESETn, Eterna loads its Fuse Table (see section 4.1.1), including setting I/O direction. In this state, Eterna checks the state of the FLASH_P_ENn and RESETn

and enters the serial flash emulation mode, if both signals are asserted. If the FLASH_P_ENn pin is not asserted but RESETn is not asserted, Eterna automatically reduces its energy consumption to a minimum until RESETn is released. Once RESETn is de-asserted, Eterna goes through a boot sequence, and then enters the Active state.

4.1.1 Fuse Table

Eterna's Fuse Table is a 2 KB page in flash that contains two data structures, one for hardware configuration immediately following Power on Reset or the assertion of RESETn and one for configuration of design specific parameters. Hardware support for configuration includes configuration of I/O, preventing I/O leakage from negatively affecting current consumption during power on, which can be a significant issue for current limited supplies. Examples of design-specific parameters include setting of UART modes, clock sources and trim values. Fuse Tables are created via the Fuse Table application software described in 040-0109 Design Specific Configuration Guide. Fuse Tables are loaded into flash using the same software and in-circuit programmer used to load Eterna's networking software image – see the 040-0110 Eterna Serial Programmer Guide for details.

4.2 Serial Flash Emulation

When both RESETn and FLASH_P_ENn are asserted, Eterna disables normal operation and enters a mode to emulate the operation of a serial flash. In this mode, its flash can be programmed with software updates. For details, see Section 2.10.

4.3 Operation

Once Eterna has completed startup, Eterna transitions to the Operational group of states (active / CPU active, active / CPU inactive, and Doze). There, Eterna cycles between the various states, automatically selecting the lowest power state possible while fulfilling the demands of network operation.

4.3.1 Active State

In Active state, the Eterna's relaxation oscillator is running and peripherals are enabled as needed. The ARM Cortex-M3 cycles as needed between CPU-active and CPU-inactive (referred to in the ARM Cortex-M3 literature as "Sleep Now" or "Sleep on Exit" modes). Eterna's extensive use of DMA and intelligent peripherals that can independently move Eterna between the Active and Doze states minimizes the time the CPU is active, significantly reducing Eterna's energy consumption.

4.3.2 Doze State

The Doze state consumes orders of magnitude less current than the Active state (see Table 6) and is entered when all of the peripherals, save the low power portion of the timer module, and the CPU are inactive. In the Doze state Eterna's full state is retained and Eterna is configured to detect, wake, and rapidly respond to activity on I/Os (such as UART signals and the TIMEn pin). The Doze state also uses the 32.768-kHz oscillator and 32 kHz based timers are active.

4.4 Duty Cycling and Autonomous Peripherals

Eterna's ability to quickly and efficiently transition between Doze and Active states, in conjunction with the ability of peripherals to operate autonomously for most operations (shown in Figure 9), enables the system solution to significantly reduce power consumption. For example the system can automatically go from Doze to Active and determine if RF energy is present. The CPU is then only woken if a packet is detected, otherwise Eterna returns to Doze mode.

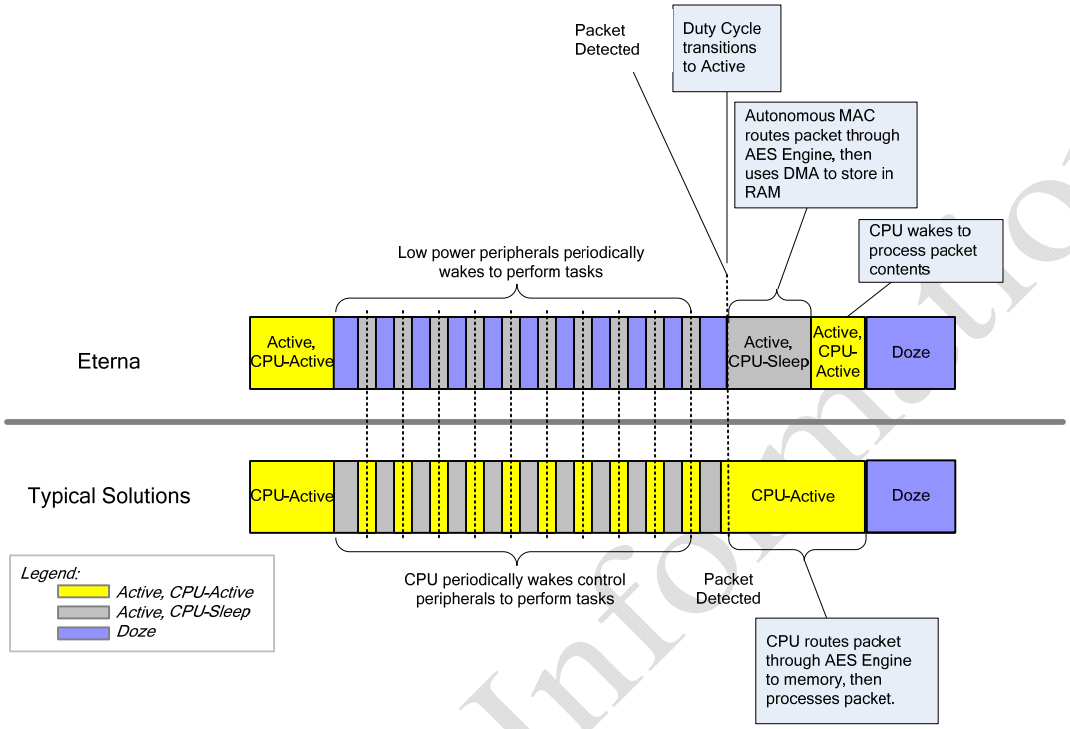


Figure 9 Low Energy Duty Cycling

5.0 Pinout

5.2 Eterna Mote Modules

The Eterna mote modules are shown in Figure 11 and Figure 12. Pins are described in Table 2, where they are grouped by function. In some cases, a pin may have multiple possible functions.

Note: All unused input pins not configured with a pull resistor (see Pull column in pin out table) must be driven to an inactive state to avoid excess leakage and undesired operation. Leakage due to floating inputs can be substantially greater than Eterna's average power consumption.

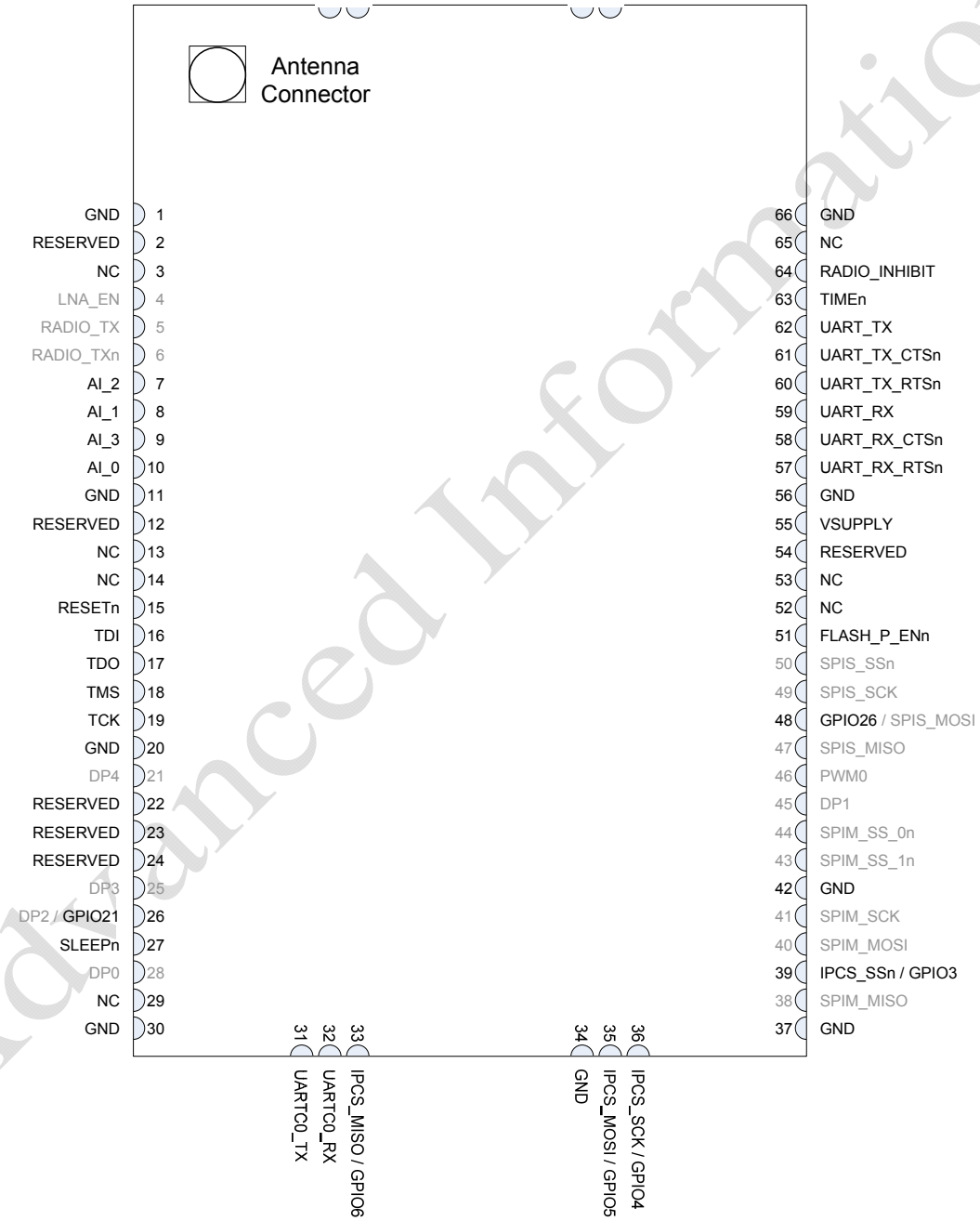


Figure 11 LTP5902-IPM – Mote Module with MMCX Antenna Connector

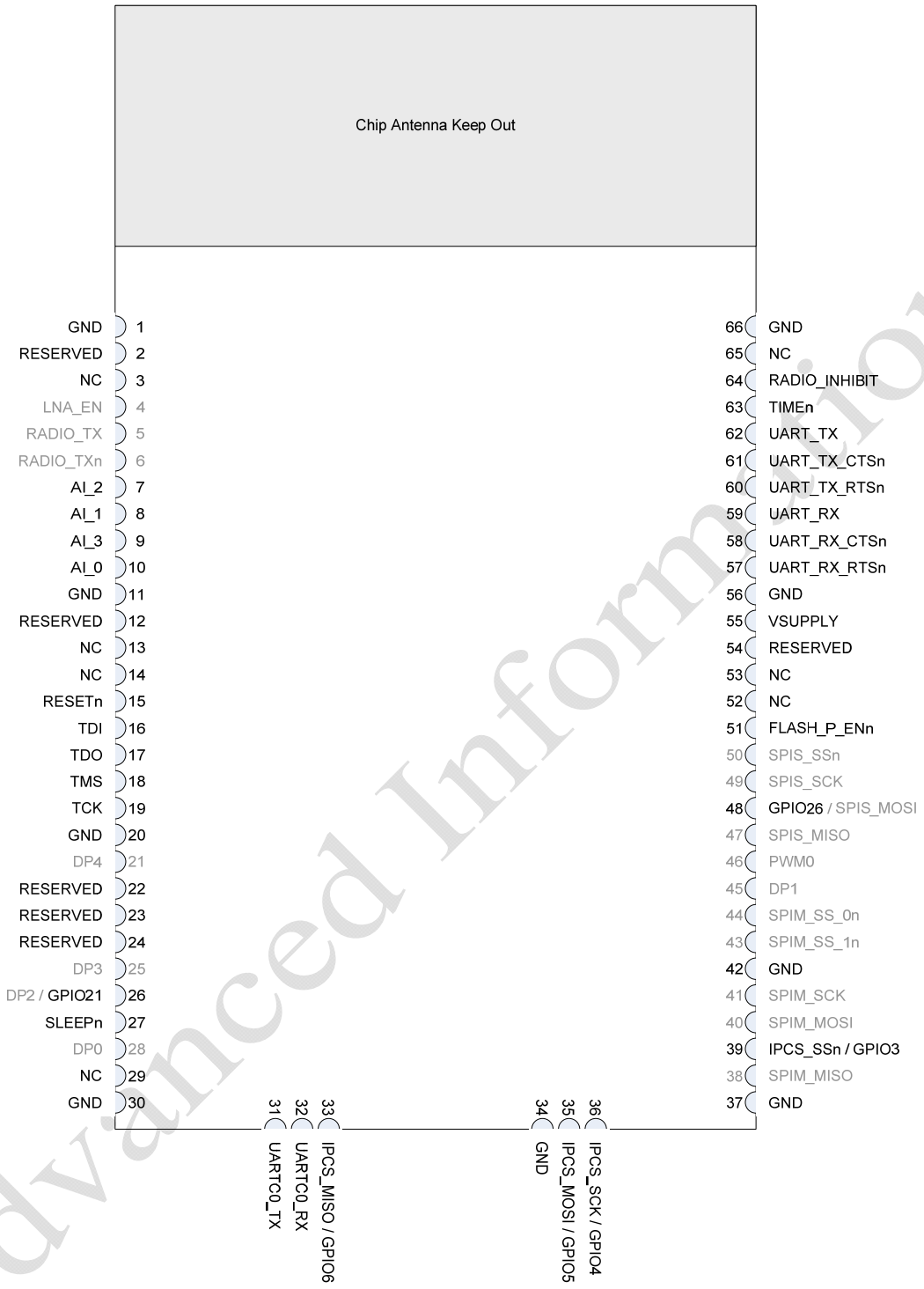


Figure 12 LTP5901-IPM – Mote Module with Chip Antenna

Table 2 *Eterna* Mote Module Pinout Assignments

	Mechanical				
NA	MECH				Contacts for mechanical support of MMCX connector
No	**Power Supply**	**Type**	**I/O**	**Pull**	**Description**
1	GND	Power	-	-	Ground
11	GND	Power	-	-	Ground
20	GND	Power	-	-	Ground
30	GND	Power	-	-	Ground
34	GND	Power	-	-	Ground
37	GND	Power	-	-	Ground
42	GND	Power	-	-	Ground
56	GND	Power	-	-	Ground
66	GND	Power	-	-	Ground
55	VSUPPLY	Power	-	-	Module power supply input
No	**Radio**	**Type**	**I/O**	**Pull**	**Description**
4	LNA_EN	1	O	-	External LNA enable
	GPIO17	1	I/O	-	General purpose digital I/O
5	RADIO_TX	1	O	-	Radio TX active (external PA enable/switch control)
	GPIO18	1	I/O	-	General purpose digital I/O
6	RADIO_TXn	1	O	-	Radio TX active (external PA enable/switch control), active low
	GPIO19	1	I/O	-	General purpose digital I/O
64	RADIO_INHIBIT	1*	I	-	Radio Inhibit
	GPIO15		I/O	-	General purpose digital I/O
No	**Analog**	**Type**	**I/O**	**Pull**	**Description**
10	AI_0	Analog	I	-	Analog input 0
8	AI_1	Analog	I	-	Analog input 1
9	AI_3	Analog	I	-	Analog input 3
7	AI_2	Analog	I	-	Analog input 2
No	**General**	**Type**	**I/O**	**Pull**	**Description**
15	RESETn	1	I	UP	Reset, Input, active low
No	**JTAG**	**Type**	**I/O**	**Pull**	**Description**
16	TDI	1	I	UP	JTAG test data in
17	TDO	1	O	-	JTAG test data out
18	TMS	1	I	UP	JTAG test mode select
19	TCK	1	I	DOWN	JTAG test clock
No	**CLI**	**Type**	**I/O**	**Pull**	**Description**
31	UARTC0_TX	2	O	-	CLI UART 0 transmit
32	UARTC0_RX	1	I	UP	CLI UART 0 receive
No	**UART**	**Type**	**I/O**	**Pull**	**Description**
57	UART_RX_RTSn	1*	I	-	UART receive (RTS) request to send, active low
58	UART_RX_CTSn	1	O	-	UART receive (CTS) clear to send, active low
59	UART_RX	1*	I	-	UART receive
60	UART_TX_RTSn	1	O	-	UART transmit (RTS) request to send, active low
61	UART_TX_CTSn	1*	I	-	UART transmit (CTS) clear to send, active low
62	UART_TX	2	O	-	UART transmit

No	IPCS SPI / FLASH Programming	Type	I/O	Pull	Description
33	IPCS_MISO	2	O	-	SPI flash emulation (MISO) master in slave out port
	GPIO6		I/O	-	General purpose digital I/O
35	IPCS_MOSI	1	I	-	SPI flash emulation (MOSI) master out slave in port
	GPIO5		I/O	-	General purpose digital I/O
36	IPCS_SCK	1	I	-	SPI flash emulation (SCK) serial clock port
	GPIO4		I/O	-	General purpose digital I/O
39	IPCS_SSn	1	I	-	SPI flash emulation slave select, active low
	GPIO3		I/O	-	General purpose digital I/O
51	FLASH_P_ENn		I	UP	Flash program enable, active low Note that this functionality is available only when RESETn is asserted
No	**Special Purpose Digital**	**Type**	**I/O**	**Pull**	**Description**
27	SLEEPn	1*	I	-	Deep Sleep, active low
63	TIMEn	1*	I	-	Time capture request, active low

* Input signals that must be driven or pulled to a valid state to avoid leakage.

5.3 Power Supply

Eterna is powered from a single pin, VSUPPLY, and generates all required supplies internally. With two integrated DC/DC converters and four voltage regulators, the sensitivity to noise on VSUPPLY is minimal. However, during typical operation Eterna will vary its load on the power supply from the µA range to 10's of mA over a few µs. During such transients, the power supply must meet the specifications for supply noise tolerance. Eterna is designed to operate with specific decoupling capacitance on VCORE, VDDA, VOSC, VDDPA, and VPRIME, as well as the internal converter capacitors C1 through C4. Failure to use correctly sized ceramic capacitors can result in supply instability and performance degradation.

5.3.1 Antenna

Eterna allows direct connection to a single-ended 50-Ohm antenna; an internal TX/RX switch simplifies external circuitry requirements. Because both the transmit and the receive paths are single-ended, a balun (with its associated cost and efficiency loss) are not required. Eterna provides options to set typical output power to 0 dBm or to +8 dBm using the on-chip PA. For further details on radio transmit and receive, see section 2.4.

5.4 Analog

Eterna has four analog inputs. Its 10-bit ADC includes a 4-bit DAC for adjusting offset and a 3-bit VGA, as shown in Figure 13. The software application layer controls ADC operation and may be configured to automatically sample any combination of the internal temperature sensor, or analog input signals.

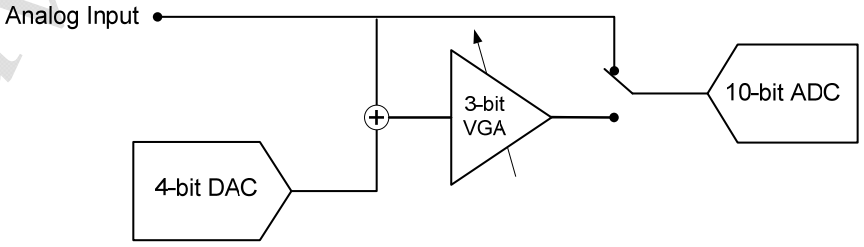


Figure 13 Analog to Digital Chain

5.5 JTAG

Eterna includes an IEEE 1149.1-compliant JTAG port for boundary scan.

6.0 Absolute Maximum Ratings

The absolute maximum ratings shown in Table 3 should not be violated under any circumstances. Permanent damage to the device may be caused by exceeding one or more of these parameters. Unless otherwise noted, all voltages in Table 3 are relative to GND.

Table 3 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units	Comments
Supply voltage (VSUPPLY to GND)	–0.3		3.76	V	
Voltage on any digital I/O pin	–0.3		VSUPPLY + 0.3 up to 3.76	V	
Input RF level			+10	dBm	Input power at antenna connector
Storage temperature range	–55		+105	°C	Extended storage at high temperature is discouraged, as this negatively affects the data retention of Eterna's calibration data.
Lead temperature			+245	°C	For 10 seconds
VSWR of antenna			3:1		
ESD protection					
Antenna pad			±8000	V	HBM
All other pads			±1000	V	HBM
			±100	V	CDM

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

7.0 Recommended Operating Conditions

Table 4 Recommended Operation Conditions

Parameter	Conditions	Min	Typ	Max	Units
VSUPPLY range	Including noise and load regulation	2.1	3.6	3.76	V
Voltage supply noise	Requires recommended RLC filter, 50 Hz to 2 MHz			250	mV_{p-p}
Operating temperature range		–40		+85	°C
Operating relative humidity	Non-condensing	10		90	% RH
Power on Reset threshold			1.5		V
Temperature ramp		-8		+8	°C/min

8.0 Electrical Characteristics

8.1 Radio Specifications

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 5 Detailed Radio Specifications

Parameter	Conditions	Min	Typ	Max	Units
Frequency Band	As specified by [1]	2.4000		2.4835	GHz
Number of channels			15		
Channel separation	As specified by [1]		5		MHz
Occupied channel bandwidth	At –20 dBc		2.7		MHz
Channel Center Frequency	Where k = 11 to 25.‡		2405 + 5 * (k-11)		MHz
Modulation	IEEE 802.15.4 DSSS				
Raw data rate	As specified by [1]		250		kbps
Range* Indoor† Outdoor† Free space	25 °C, 50% RH, +2 dBi omni-directional antenna		 100 300 1200		 m m m

* Actual RF range performance is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, and near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, actual performance varies.

† 1 meter above ground.

‡ Channel 26 as specified by [1] is not used..

8.2 DC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 6 DC Specifications

Parameter	Conditions	Min	Typ	Max	Units
Reset	After power-on reset		1.2		µA
Deep Sleep			0.8		µA
Doze	RAM on; ARM Cortex-M3, flash, radio, and peripherals off, all data and state retained, 32.768 kHz reference active		1.2		µA
Serial Flash Emulation			20		mA
Peak Operating current at +8 dBm output power	System operating at 14.7 MHz Radio Tx Flash Write			 30	 mA

Parameter	Conditions	Min	Typ	Max	Units
at 0 dBm output power				26	mA
Active*	ARM Cortex-M3, RAM, and flash on; radio and peripherals off CLK = 7.37 MHz, Vcore = 1.8 V		 2.4		 mA
Flash write	Single bank write		3		mA
Flash erase	Single bank page or mass erase		2.5		mA
Radio Tx†	Mesh Network - CLK = 7.3728 MHz, AES active 0 dBm output power +8 dBm output power		 5.4 9.7		 mA mA
Radio Rx†	Mesh Network - CLK = 7.3728 MHz, AES active		 4.5		 mA

Note: See section 3.0 for detailed operational definitions of states.

* CLK = Clock frequency of CPU and peripherals.

† Current with autonomous MAC handling packet transmission and reception; CPU idle.

8.3 Radio Receive Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 7 Radio Receive Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Receiver sensitivity	PER = 1%, as specified by [1]		–93		dBm
Receiver sensitivity	PER = 50%		–95		dBm
Saturation (maximum input level)			0		dBm
Adjacent channel rejection (high side)	Desired signal at -82 dBm, adjacent modulated channel at 5 MHz, PER = 1%, as specified by [1]		22		dBc
Adjacent channel rejection (low side)	Desired signal at -82 dBm, adjacent modulated channel at -5 MHz, PER = 1%, as specified by [1]		19		dBc
Alternate channel rejection (high side)	Desired signal at -82 dBm, adjacent modulated channel at 10 MHz, PER = 1%, as specified by [1]		40		dBc
Alternate channel rejection (low side)	Desired signal at -82 dBm, adjacent modulated channel at -10 MHz, PER = 1%, as specified by [1]		36		dBc
Second alternate channel rejection	Desired signal at -82 dBm, adjacent modulated channel at +/-10 MHz, PER = 1%, as specified by [1]		42		dBc
Co-channel rejection	Desired signal at -82 dBm. Undesired signal is 802.15.4 modulated at same frequency. PER = 1%, as specified by [1]		–6		dBc
LO feed through			<–55		dBm
Frequency error tolerance	[1] requires ±40		±50		ppm
Symbol rate error tolerance			±50		ppm
RSSI input range			–10 to –90		dBm
RSSI accuracy			±6		dB
RSSI resolution			1		dB

8.4 Radio Transmitter Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 8 Radio Transmitter Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Output power Calibrated settings	Delivered to a 50 Ω load, over temperature and voltage ranges		 0 +8		 dBm dBm
Spurious emissions 30 MHz to 1000 MHz 1 GHz to 12.75 GHz Upper Band Edge (Peak) Upper Band Edge (Average) Lower Band Edge	Conducted measurement with a 50 Ω single-ended load, +8 dBm output power. All measurements made with Max Hold. RF implementation per Eterna reference design. RBW = 120 kHz, VBW = 100 Hz RBW = 1 MHz, VBW = 3 MHz RBW = 1 MHz, VBW = 3 MHz RBW = 1 MHz, VBW = 10 Hz RBW = 100 kHz, VBW = 100 kHz		 <–70 –45 -37 -49 -45		 dBm dBm dBm dBm dBc
Harmonic emissions 2nd Harmonic 3rd Harmonic	Conducted measurement delivered to a 50 Ω load, Resolution Bandwidth = 1 MHz, Video Bandwidth = 1 MHz, RF implementation per Eterna reference design		 –50 –45		dBm

8.5 Digital I/O Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 9 Digital I/O Type 1

Parameter	Conditions	Min	Typ	Max	Units
V_{IL} (low-level input voltage)		–0.3		0.6	V
V_{IH} (high-level input voltage)		VSUPPLY - 0.3†		VSUPPLY + 0.3†	V
V_{OL} (low-level output voltage)	$I_{OL(max)}$ = 1.2 mA			0.4	V
V_{OH} (high-level output voltage)	$I_{OH(max)}$ = −1.8 mA	VSUPPLY - 0.3†		VSUPPLY + 0.3†	V
Input leakage current	pull-up / pull-down pins disabled.		50		nA
† Min and Min and Max IO input levels must respect the Minimum and Maximum voltages for VSUPPLY.					

Table 10 Digital I/O Type 2

Parameter	Conditions	Min	Typ	Max	Units
V_{IL} (low-level input voltage)		–0.3		0.6	V
V_{IH} (high-level input voltage)		VSUPPLY - 0.3†		VSUPPLY + 0.3†	V
V_{OL} (low-level output voltage) Low Drive	$I_{OL(max)}$ = 2.2 mA			0.4	V
V_{OH} (high-level output voltage) Low Drive	$I_{OH(max)}$ = −3.2 mA	VSUPPLY - 0.3†		VSUPPLY + 0.3†	V
V_{OL} (low-level output voltage) High Drive	$I_{O(max)}$ = 4.5 mA			0.4	V
V_{OH} (high-level output voltage)	$I_{OH(max)}$ = −6.3 mA	VSUPPLY		VSUPPLY	V

High Drive		- 0.3†		+ 0.3†	
Input leakage current			50		nA
† Min and Min and Max IO input levels must respect the Minimum and Maximum voltages for VSUPPLY.					

8.6 Temperature Sensor Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 11 Temperature Sensor Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Offset	Temperature offset error at 25 ºC		±0.25		°C
Slope error	Slope error from -40 to +85 ºC		±0.033		°C/°C

8.7 ADC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 12 ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Variable gain amplifier Gain Gain error		 1		 8 1	 %
Digital to analog converter (DAC) Offset output Differential non-linearity (DNL)		 1.8/16		 1.8 7.2	 V mV
Analog to digital converter (ADC) Full-scale, signal Resolution Offset Differential non-linearity (DNL) Integral non-linearity (INL) Settling time Conversion time Current consumption	 Midscale 10-kOhm source impedance 		 1.80 1.8 	 ±4 1 1 10 20 50	 V mV LSB LSB LSB µs µs µA
Analog Inputs* Load Input resistance			 17 1	 35 2	 pF kOhm
* The analog inputs to the ADC can be model as a series resistor to a load capacitor. At a minimum the entire circuit, including the source impedance for the signal driving the analog input should be designed to settle to within ¼ LSB within the sampling window to match the performance of the ADC.					

8.8 System Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 13 System Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Doze to Active state delay			5		µs
Doze to Radio TX or RX			1.2		ms
Q_{CCA} charge to sample RF channel	Start from Doze state		4		µC
Radio baud rate			250		kbps
RESETn pulse width		125			µs

8.9 UART AC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 14 UART Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
t_{RX_BAUD}	Deviation from baud rate	–2		+2	%
t_{TX_BAUD}	Deviation from baud rate	–1		+1	%
$t_{RX\_RTS\_R\ to\ RX\_CTS}$	Assertion of UART_RX_RTSn to assertion of UART_RX_CTSn, or negation of UART_RX_RTSn to negation of UART_RX_CTSn	0		22	ms
$t_{CTS\_R\ to\ RX}$	Assertion of UART_RX_CTSn to start of byte	0		20	ms
$t_{EOP\ to\ RX\_RTS}$	End of packet (end of the last stop bit) to negation of UART_RX_RTSn	0		22	ms
$t_{TX\_RTS\_T\ to\ TX\_CTS}$	Assertion of UART_TX_RTSn to assertion of UART_TX_CTSn, or negation of UART_TX_RTSn to negation of UART_TX_CTSn	0		22	ms
$t_{TX\_CTS\_T\ to\ TX}$	Assertion of UART_TX_CTSn to start of byte	0		2	bit period
$t_{EOP\ to\ TX\_RTS}$	End of packet (end of the last stop bit) to negation of UART_TX_RTSn	0		1	bit period
$t_{RX\_INTERBYTE}$	Receive Inter-byte delay			100	ms
$t_{TX\ to\ TX\_CTS}$	Start of byte to negation of UART_TX_CTSn	0			ms
$t_{INTERPACKET}$	Transmit and Receive Inter-packet delay (Mode 4 only)	100			ms

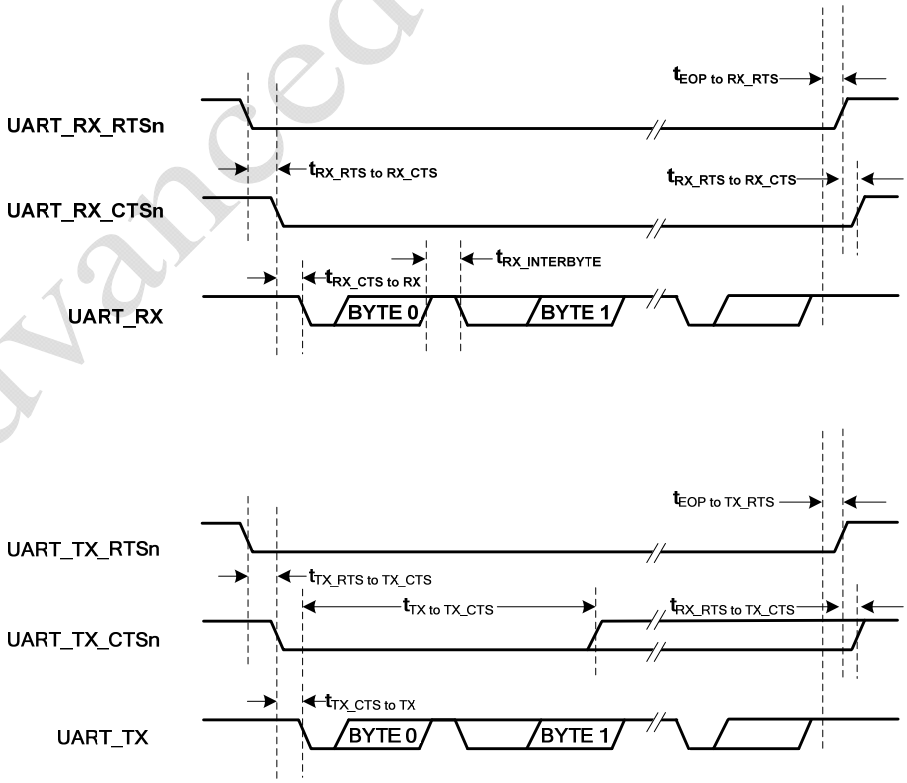


Figure 16 UART Timing

8.10 TIMEn AC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified. Note that the time pin must remain negated until the time packet has been received.

Table 15 Timestamp Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
t_{strobe}		125			µs
$t_{response}$	From rising edge of TIMEn			100	ms
Resolution	See the serial API definition for getParameter<time>		+/- 1		µs
Network-wide time accuracy	Stable temperature environment		+/- 5		µs

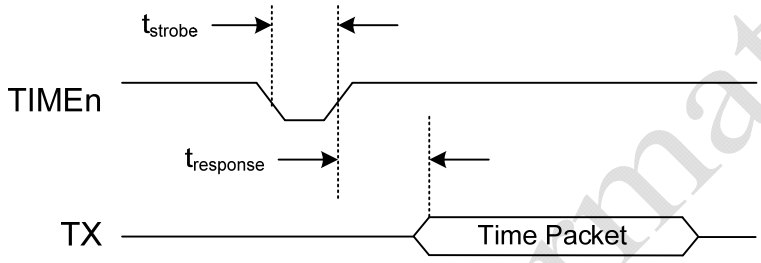


Figure 17 Timestamp Timing Diagram

8.11 SLEEPn AC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified. Note that the time pin must remain negated until the time packet has been received.

Table 16 SLEEPn Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
t_{doze}	From falling edge of SLEEPn			20	ms
T_{sleep_strobe}	Maximum strobe width			2	s

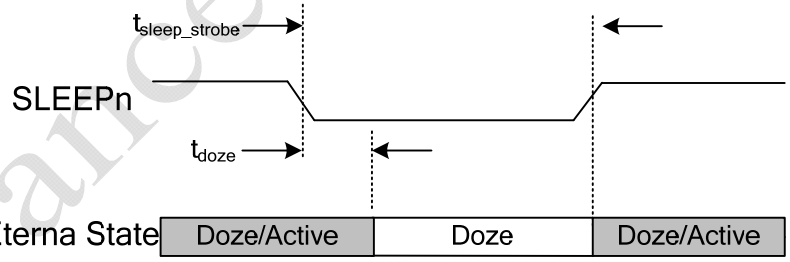


Figure 18 SLEEPn Timing Diagram

8.12 RADIO_INHIBIT AC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified. Note that the time pin must remain negated until the time packet has been received.

Table 17 RADIO_INHIBIT Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
t_{radio_off}	From rising edge of RADIO_INHIBIT			20	ms
$T_{radio\_inhibit\_strobe}$	Maximum strobe width			2	s

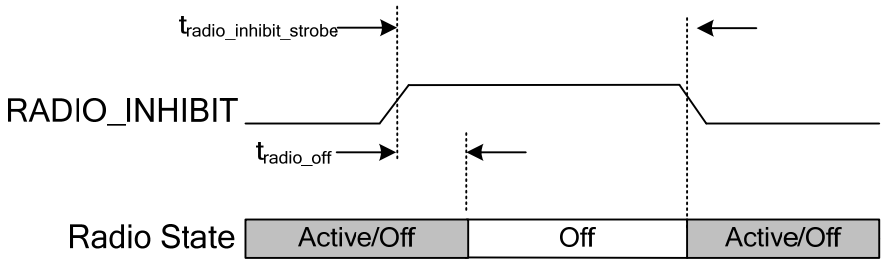


Figure 19 RADIO_INHIBIT Timing Diagram

8.13 FLASH AC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C, unless otherwise specified.

Table 18 FLASH AC Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
$t_{32\text{-}BIT\_WORD}$	Writing a 32-bit word			21	µs
t_{PAGE_ERASE}	Page Erase			21	ms
t_{MASS_ERASE}	Bank Erase			21	ms

8.14 Flash Programming AC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at 25 °C with 10 pF load capacitance, unless otherwise specified.

Table 19 SPI Slave AC Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
t_{SSS}	IPCS_SSn setup to leading edge of IPCS_SCK	15			ns
t_{SSH}	IPCS_SSn hold from trailing edge of IPCS_SCK	15			ns
t_{CK}	IPCS_SCK period	50			ns
t_{DIS}	IPCS_MOSI data setup	15			ns
t_{DIH}	IPCS_MOSI data hold	5			ns
t_{DOV}	IPCS_MISO data valid	3		15	ns
t_{OFF}	IPCS_MISO data tri-state	0		15	ns

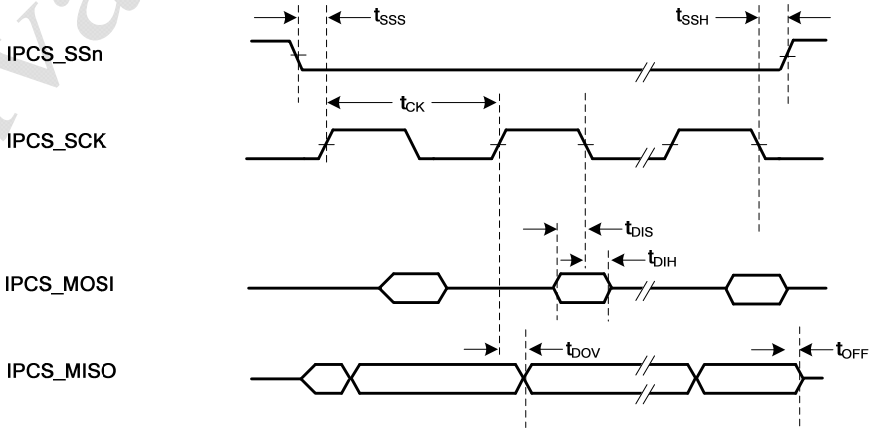
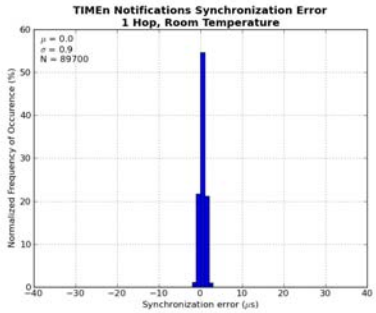
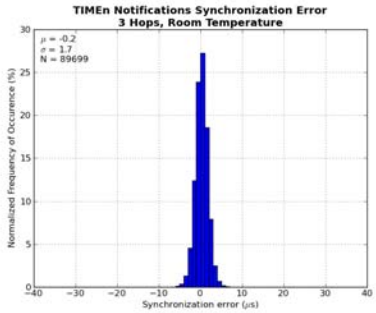


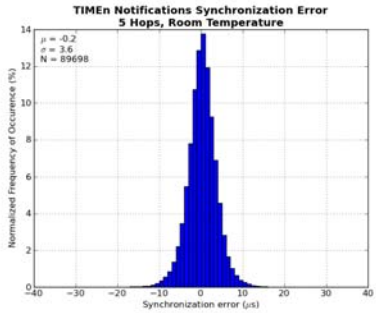
Figure 20 Flash Programming Slave Timing

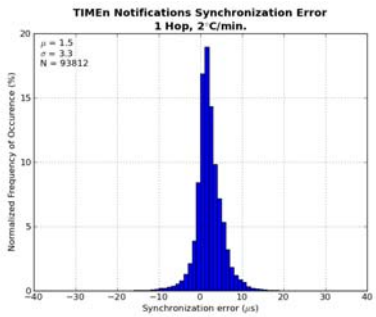
9.0 Typical Performance Characteristics

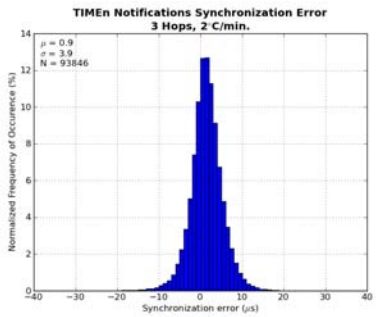
All TIMEn synchronization error testing was performed with the hop-1 mote inside a temperature chamber. Timing errors due to temperature changes and temperature differences both between the AP and this mote and between this mote and its descendents therefore propagated down through the network. The synchronization of the hop-3 and hop-5 motes to the AP was then affected by the temperature ramps even though they were at room temperature. For 2°C/min. testing the temperature chamber was cycled between -40°C and 85°C at this rate for 24 hours. For 8°C/min. testing, the temperature chamber was rapidly cycled between 85°C and about 45°C for 8 hours, followed by rapid cycling between -5°C and about 45°C for 8 hours, and lastly, rapid cycling between -40°C and about 15°C for 8 hours..

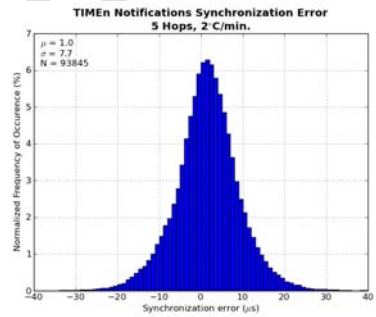


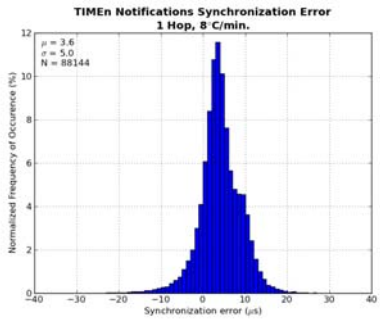


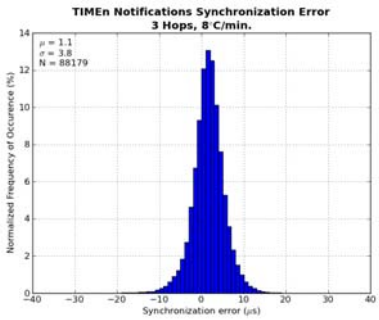


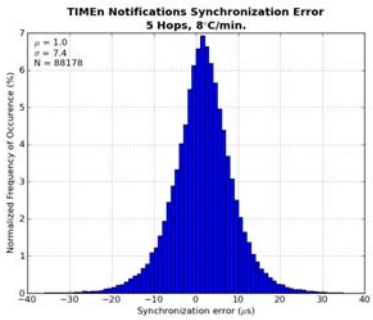












Network motes typically route through at least two parents traffic destined for the manager. The bandwidth and keep-alive overhead required to support network motes will be shared across all of the mote's parents. The supply current plots include a parameter called traffic-weighted descendants. In these graphs the term traffic-weighted descendants refers to an amount of activity equivalent to the number of descendants were all of the network traffic and keep-alives directed to the mote in question. Generally the number of descendants of a parent is more (typically 2x or more) than the number of traffic-weighted descendants. For example, with reference to Figure 25 mote P1 has 0.75 traffic-weighted descendants. To obtain this value notice that mote D1 routes half its packets through mote P1 adding 0.5 to the traffic-weighted descendant value; the other half of D1's traffic is routed through its other parent, P2. Mote D2 routes half its packets through mote D1 (the other half going through parent P3), which we know routes half its packets to mote P1, adding another 0.25 to the traffic-weighted descendant value for a total traffic-weighted descendant value of 0.75.

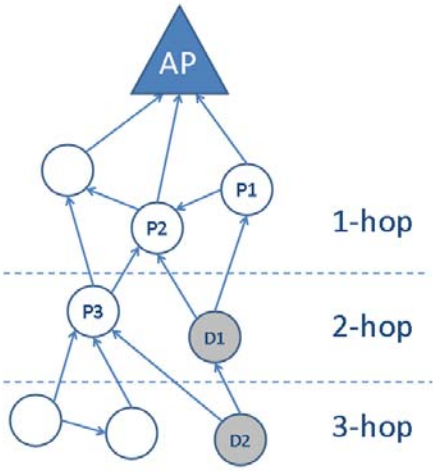
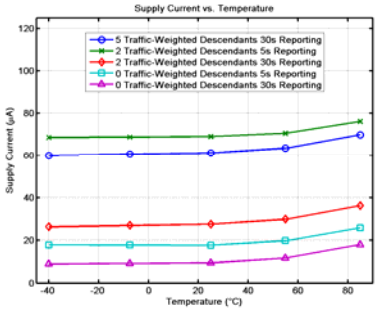
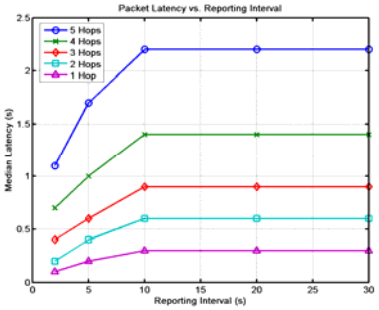
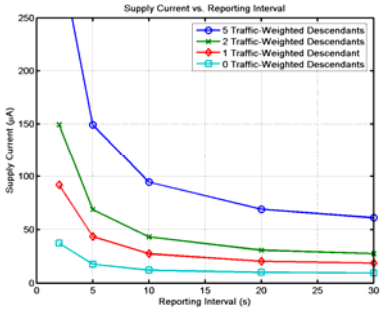


Figure 25 Network Graph Depicting Traffic Weighted Descendant Value Calculation

The following plots correspond to networks with 1024 slots/frame, an assumed path stability of 80%, an 80 byte packet and unless otherwise specified operation at 25 degrees C.







10.0 Mechanical Details

10.2 Mote Module

The Eterna mote modules comes in 66-lead, 1 mm lead pitch castellated PCB, as illustrated in Figure 27 and in Figure 28.

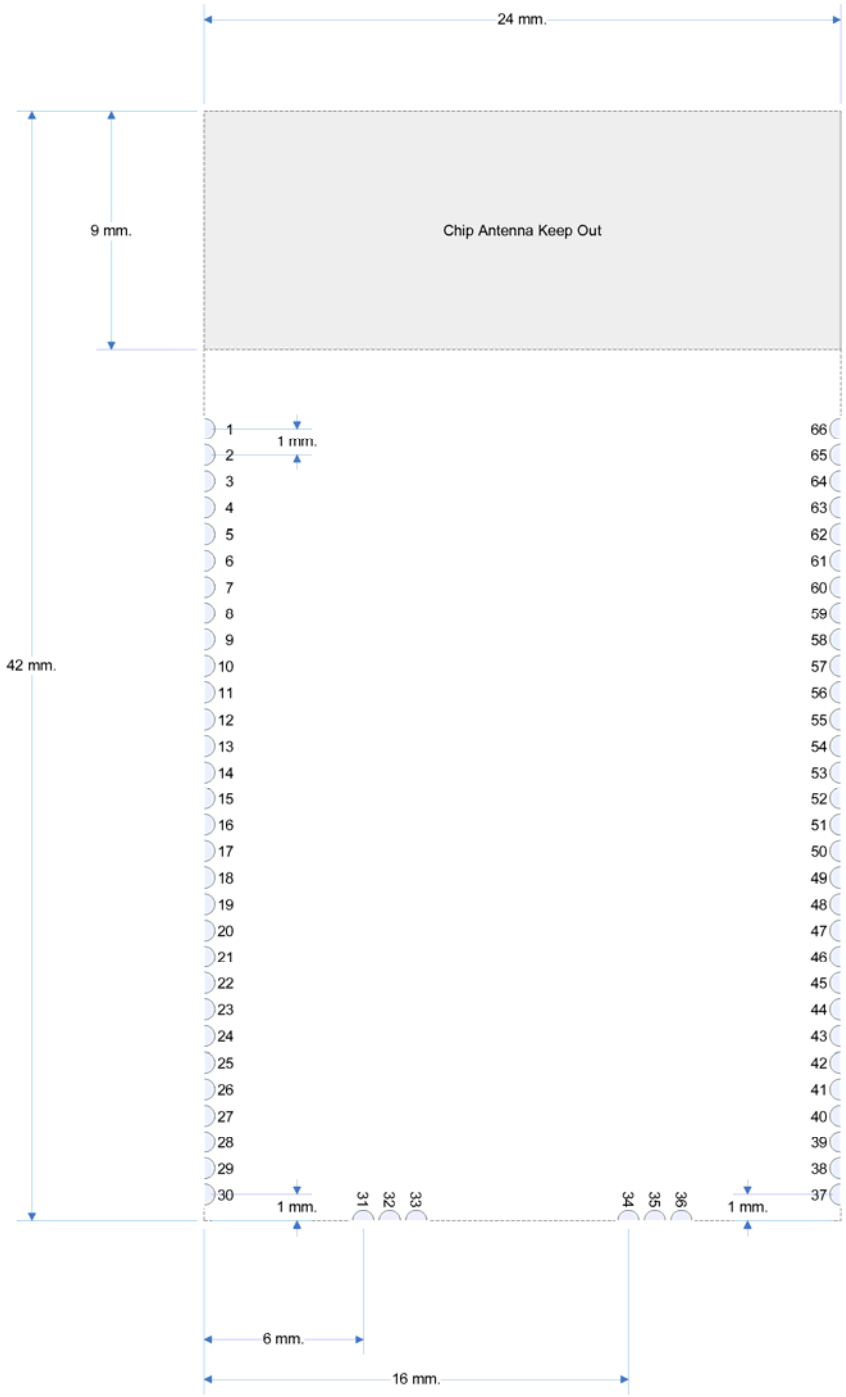


Figure 27 Mechanical Drawing – LTP5901

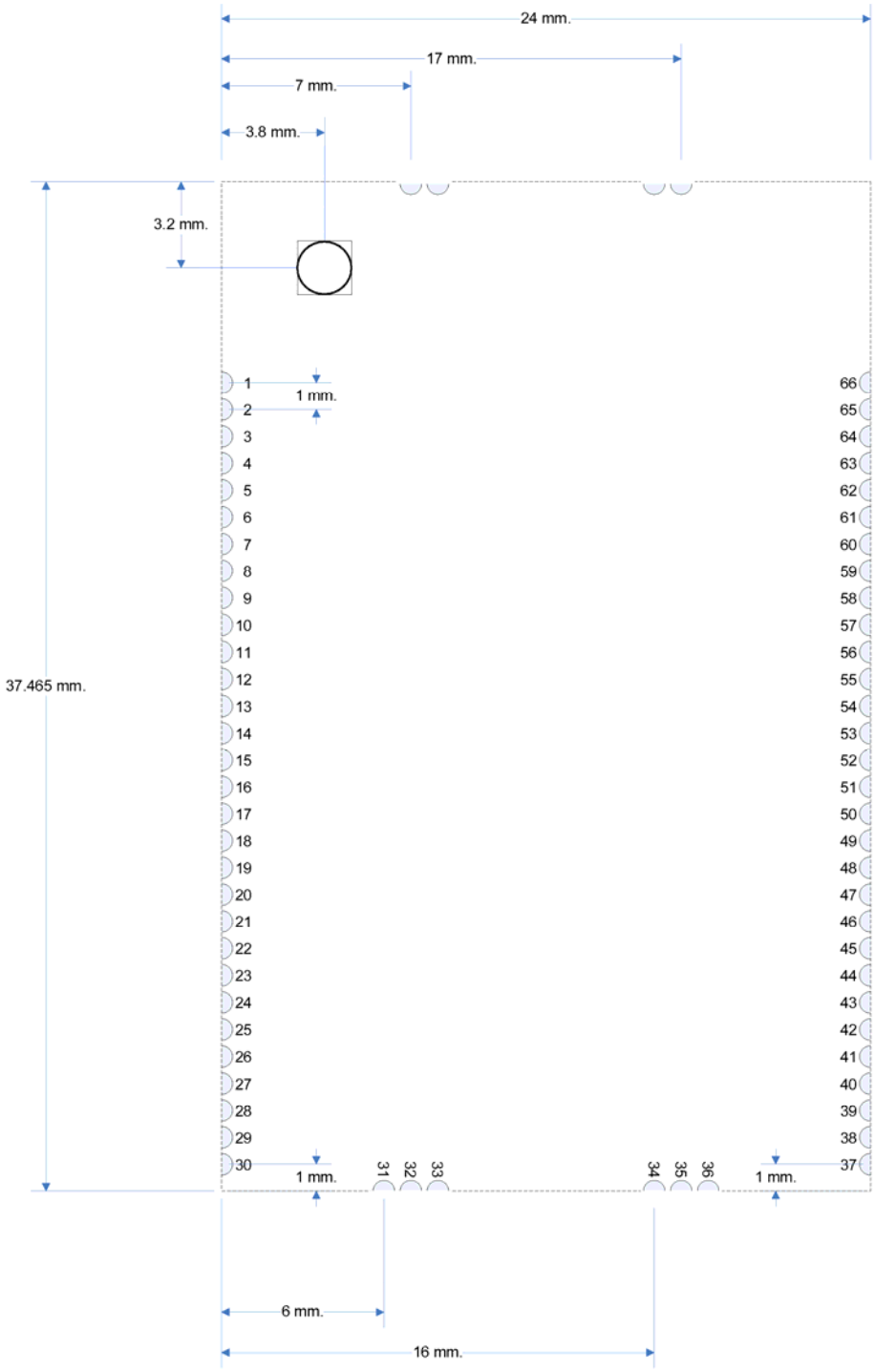


Figure 28 Mechanical Drawing – LTP5902

10.3 Soldering Information

Eterna is suitable for both eutectic PbSn and RoHS-6 reflow. The maximum reflow soldering temperature is 260 ºC.

11.0 Regulatory and Standards Compliance

LTP5901 is compliant with EU, FCC and IC radio frequency regulations. For specific information on regulations, test procedures, and labeling requirements, see the "LTP5901 Regulatory User Guide".

LTP5902 is compliant with EU, FCC and IC radio frequency regulations. For specific information on regulations, test procedures, and labeling requirements, see the "LTP5902 Regulatory User Guide".

11.1 Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances (RoHS) is a directive that places maximum concentration limits on the use of cadmium (Cd), lead (Pb), hexavalent chromium (Cr+6), mercury (Hg), Polybrominated Biphenyl (PBB), and Polybrominated Diphenyl Ethers (PBDE). Dust Networks is committed to meeting the requirements of the European Community directive 2002/95/EC.

This product has been specifically designed to utilize RoHS-compliant materials and to eliminate or reduce the use of restricted materials to comply with 2002/95/EC.

The RoHS-compliant design features include:

- RoHS-compliant solder for solder joints
- RoHS-compliant base metal alloys
- RoHS-compliant precious metal plating
- RoHS-compliant cable assemblies and connector choices
- Lead-free QFN package
- Halogen-free mold compound
- RoHS-compliant and 245 °C re-flow compatible

Note: Customers may elect to use certain types of lead-free solder alloys in accordance with the European Community directive 2002/95/EC. Depending on the type of solder paste chosen, a corresponding process change to optimize reflow temperatures may be required.

12.0 References

[1] IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf

13.0 Order Information

LEAD FREE FINISH**	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTP5901IPC-IPMA???#PBF	LTP5901	66-Lead (37.465mm x 24mm) PCB	-40 °C to 85 °C
LTP5902IPC-IPMA???#PBF	LTP5902	66-Lead (42mm x 24mm) PCB	-40 °C to 85 °C

** See http://www.linear.com/ or contact your sales representative to determine the three digit software version field, ???.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

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